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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/993,993	11/14/2001	Shunpei Yamazaki	SEL 291	9060

7590 06/30/2004

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EXAMINER	
TRAN, MINH LOAN	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 06/30/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/993,993	YAMAZAKI ET AL.	
	Examiner	Art Unit	
	Minh-Loan T. Tran	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 April 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-36* is/are pending in the application.

4a) Of the above claim(s) *20-36* is/are withdrawn from consideration.

5)☒ Claim(s) *16 and 17* is/are allowed.

6)☒ Claim(s) *1-7,11,12,15,18 and 19* is/are rejected.

7)☒ Claim(s) *8-10,13 and 14* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4/07/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statement filed on 4/07/2004 has been considered.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-7, 11, 12, 15, 18, 19 stand rejected under 35 U.S.C. 103(a) as being obvious over Suzawa et al. (6,515,336) as the reasons set forth in the Office Action mailed on 11/25/2003.

The applied reference has a common inventor with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art only under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 103(a) might be overcome by: (1) a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not an invention " by another" ; (2) a showing of a date of invention for the claimed subject matter of the application which corresponds to subject matter disclosed but not claimed

in the reference, prior to the effective U.S. filing date of the reference under 37 CFR 1.131; or (3) an oath or declaration under 37 CFR 1.130 stating that the application and reference are currently owned by the same party and that the inventor named in the application is the prior inventor under 35 U.S.C. 104, together with a terminal disclaimer in accordance with 37 CFR 1.321(c). For applications filed on or after November 29, 1999, this rejection might also be overcome by showing that the subject matter of the reference and the claimed invention were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person. See MPEP § 706.02(l)(1) and § 706.02(l)(2).

With regard to claims 1, 11, figures 1A-1D, 2A-2D, 3A-3C, 4A, 4B, 19A-19E of Suzawa et al. disclose a semiconductor device comprising at least a pixel portion and a driver circuit portion, the semiconductor device comprising a plurality of TFTS and each of TFTS comprising:

a semiconductor layer 103a formed on an insulating surface;

an insulating film 109 formed on the semiconductor layer 103a ; and

a gate electrode 110, 111 formed on the insulating film 109;

wherein the pixel portion comprises at least one TFT and the driving circuit portion has at least an n-channel TFT 201a and a p-channel TFT 200a;

wherein a gate electrode 119f of the n-channel TFT of the driving circuit portion has a laminate structure with a first conductive layer 119e as a lower layer and a second conductive layer 119d as an upper layer, the first conductive layer 119e having a first width and a second conductive layer 119d having a second width that is narrower than the first width, and

wherein a gate electrode 122f of the TFT of at least the pixel portion has a laminate structure comprising a first conductive layer 122d and a second conductive layer 122e, an upper surface of the first conductive layer 122d and a lower surface of the second conductive layer 122e having the same width.

Figures 1A-1D, 2A-2D, 3A-3C, 4A, 4B of Suzawa et al. do not disclose the TFT of the pixel portion is a P-channel TFT. However, it would have been obvious to one of ordinary skill in the art to replace the NTFT by the PTFT because the NTFT and PTFT can be interchanged. Note Yamazaki (US 2001/0014535), figure 6 and paragraph [0077] , is cited to support for the well known position.

With regard to claim 2, figures 1A-1D, 2A-2D, 3A-3C, 4A, 4B of Suzawa et al. show the edge of the first conductive layer 119e of the n-channel TFT of the driving circuit portion is tapered in section.

With regard to claim 3, figures 1A-1D, 2A-2D, 3A-3C, 4A, 4B of Suzawa et al. show the p-channel TFT of the pixel portion comprises a plurality of channel forming regions 222a, 222b, 228.

With regard to claim 4, figures 1A-1D, 2A-2D, 3A-3C, 4A, 4B of Suzawa et al. show the n-channel TFT 201a of the driving circuit portion, the gate electrode has a tapered portion, and the semiconductor layer comprises a channel forming region overlapping the gate electrode and an impurity region partially overlapping the gate electrode.

With regard to claim 5, figures 1A-1D, 2A-2D, 3A-3C, 4A, 4B of Suzawa et al. show the impurity region of the n-channel TFT 201a has a region that has an impurity concentration gradient in a range of at least 1×10^{16} to 1×10^{19} atoms/cm^3, and the impurity concentration thereof increases as the distance from the channel forming region 210 increases.

With regard to claim 6, figures 1A-1D, 2A-2D, 3A-3C, 4A, 4B of Suzawa et al. show the impurity region of the n-channel TFT 201a includes a source region 213 or a drain region 212.

With regard to claim 7, figures 1A-1D, 2A-2D, 3A-3C, 4A, 4B of Suzawa et al. show the TFT 204 of the pixel region has an LDD region 223a between the channel

forming region 222a and a source region 225, or between the channel forming region 222a and a drain region 226.

With regard to claims 12, 15, figures 1A-1D, 2A-2D, 3A-3C, 4A, 4B,19A-19E of Suzawa et al. disclose a semiconductor device comprising at least a pixel portion and a driver circuit portion, the semiconductor device comprising a plurality of TFTS and each of TFTS comprising:

a semiconductor layer 103a formed on an insulating surface;

an insulating film 109 formed on the semiconductor layer 103a, and

a gate electrode 110, 111 formed on the insulating film 109;

wherein the pixel portion comprises at least one TFT 204 and the driving circuit portion has at least an n-channel TFT 201a and a p-channel TFT 200a;

wherein in the TFT 204 of the pixel portion, the gate electrode has a tapered portion, and the semiconductor layer comprises a plurality of channel forming regions 222a overlapping the gate electrode 122f and an impurity region 223a partially overlapping the gate electrode 122f, and wherein in the n-channel TFT 201a of the driving circuit portion, the gate electrode has a tapered portion, and the semiconductor layer comprises a channel fonning region 210 overlapping the gate electrode and an impurity region 211 partially overlapping the gate electrode.

Figures 1A-1D, 2A-2D, 3A-3C, 4A, 4B of Suzawa et al. do not disclose the TFT of the pixel portion is a P-channel TFT. However, it would have been obvious to one of ordinary skill in the art to replace the NTFT by the PTFT because the NTFT and PTFT can be interchanged. Note Yamazaki (US 2001/0014535), figure 6 and paragraph [0077] , is cited to support for the well known position.

With regard to claims 18 and 19, figures 1A-1D, 2A-2D, 3A-3C, 4A, 4B, 19A-19E of Suzawa et al. further disclose the pixel portion comprises an electrode 148a, 148b formed on the second insulating film 143 and connected to the impurity region 225 of the TFT of the pixel portion; and a pixel electrode153a, 153b formed on the second insulating film 143 and comprising the same material as the electrode 148a, 148b.

Figures 1A-1D, 2A-2D, 3A-3C, 4A, 4B, 19A-19E of Suzawa et al. do not disclose the TFT of the pixel portion is a P-channel TFT. However, it would have been obvious to one of ordinary skill in the art to replace the NTFT by the PTFT because the NTFT and PTFT can be interchanged. Note Yamazaki (US 2001/0014535), figure 6 and paragraph [0077] , is cited to support for the well known position.

Allowable Subject Matter

3. Claims 8-10, 13, 14 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

4. Claims 16, 17 are allowable over the references of record because none of these references disclose or can be combined to yield the claimed invention such as the gate wiring line comprises the same material as a pixel electrode connected to the impurity region of the p-channel TFT of the pixel portion.

Response to Arguments

5. Applicant's arguments filed 4/07/2004 have been fully considered but they are not persuasive.

It is argued, at page 2 of the remarks, that " there must be some teaching, suggestion or motivation in order to modify a references to arrive at the claimed invention. " However, in response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves **or in the knowledge generally available to one of ordinary skill in the art.** See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, Yamazaki (US 2001/0014535), figure 6 and paragraph [0077] , does disclose that the N-TFT of the pixel portion can be replaced by the P-TFT because the N-TFT and P-TFT can be interchanged.

Conclusion

6. THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Minh-Loan T. Tran whose telephone number is (571) 272-1922. The examiner can normally be reached on Monday-Friday 9:00 AM-5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner' s supervisor, Nathan J. Flynn can be reached on (571) 272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Mlt

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Art Unit 2826